PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Sirichotiyakul et al.**	§	**Group Art Unit: 2123**
Serial No.: 09/580,854	§	**Examiner: Thangavelu, Kandasamy**
Filed: May 30, 1999	§	**Attorney Docket No. SC91051A**
Title: Methods for Analyzing Integrated Circuits and Apparatus Therefor	§	**Freescale Semiconductor, Inc.** **Law Department** **7700 West Parmer Lane, MD:TX32/PL02** **Austin, TX 78729**

DECLARATION UNDER 37 C.F.R. § 1.131

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Tim Edwards declares as follows:

1. I am an Applicant for the patent application entitled "Methods for Analyzing Integrated Circuits and Apparatus Therefor," Serial No. 09/580,854, filed May 30, 2000, and an inventor of the subject matter described and claimed therein.

2. Prior to the publication of "Stand-by power minimization through simultaneous threshold voltage selection and circuit sizing," authored by myself and others in 1999, I completed and reduced to practice, in the United States of America, the invention described and claimed in the subject application, as evidenced by the following:

   a) I, along with my co-inventors, submitted two Motorola Disclosure Forms numbered 91051 and 91052, attached as Exhibits A and B hereto, which describe the invention described and claimed in the subject application. My signature, provided at the time

these disclosures were submitted, appears on both of these disclosure forms. These disclosure forms were kept in confidence and not published or disclosed to the public.

3. Each of the dates deleted from Exhibits A and B is prior to the publication of "Stand-by power minimization through simultaneous threshold voltage selection and circuit sizing," first published by myself and my co-authors in an ACM proceeding in 1999.

4. I further declare that all statements made herein of my own knowledge and all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful and false statements and the like so made are punishable by fine or imprisonment or both under § 1001 of Title 18 of United States Code and that such willful and false statements may jeopardize the validity of the above-referenced application and any patent issuing therefrom.

FURTHER DECLARANT SAYETH NOT.

Tim Edwards

Date: Feb 7, 2005